

WinPath2 and UFE3

WINPATH™ ACCESS PACKET PROCESSORS

Highlights

Together, the Win86xM6 and the UFE3 offer a two-chip, programmable protocol solution. Termination and Interworking features are customized to meet the exact needs of the Multi-Service Access Market.

- Provides fully channelized OC12 support (scalable to OC 48 with multiple devices) for the most popular Multi-Service protocols, down to DS0 granularity, for a total of 8064 DS0.
- These devices combined offer the following factory verified protocols: FR, MFR, ATM-UNI, ATM-IMA, ATM-CES (structured and unstructured), PPP, MLPPP, HDLC, FR to ATM interworking, PWE3-ATM, PWE3-HDLC, SAToP, CESoPSN, and adaptive and differential clock recovery
- Available IP cores for UFE3 FPGA in source or object formats
- Data Path protocols provided to customer in a ready- to-use format that can operate simultaneously on different ports
- Communications throughput over 4M pps
- The Data and Control Path functions are incorporated in a single, highly programmable packet processor for cost efficiency and flexibility
- Memory configurations can be tuned to support a range of diverse applications
- Datapath software is programmed as uni-processor in C for fastest time to market and is managed by up to six engines
- Wintegra's custom programming, including more than 100 examples, is available through an extensive suite of development tools.

Multi-Service Access – Any Service, Any Port:

WinPath2™ is the most advanced semiconductor product family Wintegra offers to-date. WinPath2 offers designers a comprehensive method to handle the data path with numerous devices targeted for the Access Infrastructure. ATM and IP can be selected independently as a transport protocol per port. A full set of IP services, including ATM, PPP and Ethernet, may be offered over any L2 protocol. The software enables any port to instantly migrate from ATM to IP transport with zero hardware changes.

With the addition of the WIN867M6, WIN860M6 and UFE3 devices, Wintegra strengthens its family of devices focused on the Multi-Service Access (MSA) market, providing an industry leading mix of high-performance hardware and advanced, time-saving software features customized for the MSA market space.

The WIN867M6 has an on-board MIPS 24KC core, while the WIN860M6 uses an external PowerPC processor for control path operations. Each device can be used in conjunction with Wintegra's UFE3 (Universal Front End) and bundled with a rich set of MSA-focused protocols. These include: Frame Relay, Multi-link Frame Relay, ATM-UNI, Inverse Muxing for ATM (ATM IMA), ATM Circuit Emulation Services (CES), PPP, Multi-link PPP, multi-channel HDLC, PWE3-ATM, PWE3-HDLC, SAToP, CESoPSN, and adaptive and differential clock recovery .

WinPath complements this complete protocol offering with comprehensive support, a feature that is increasingly important in MSA equipment designs.

Extensible Performance Architecture:

With the WIN86xM6 devices plus UFE3, Wintegra provides fully channelized OC12 MSA support .

Typical Applications:

A line card designed with the Win867/UFE3 is shown below. This line card would support:

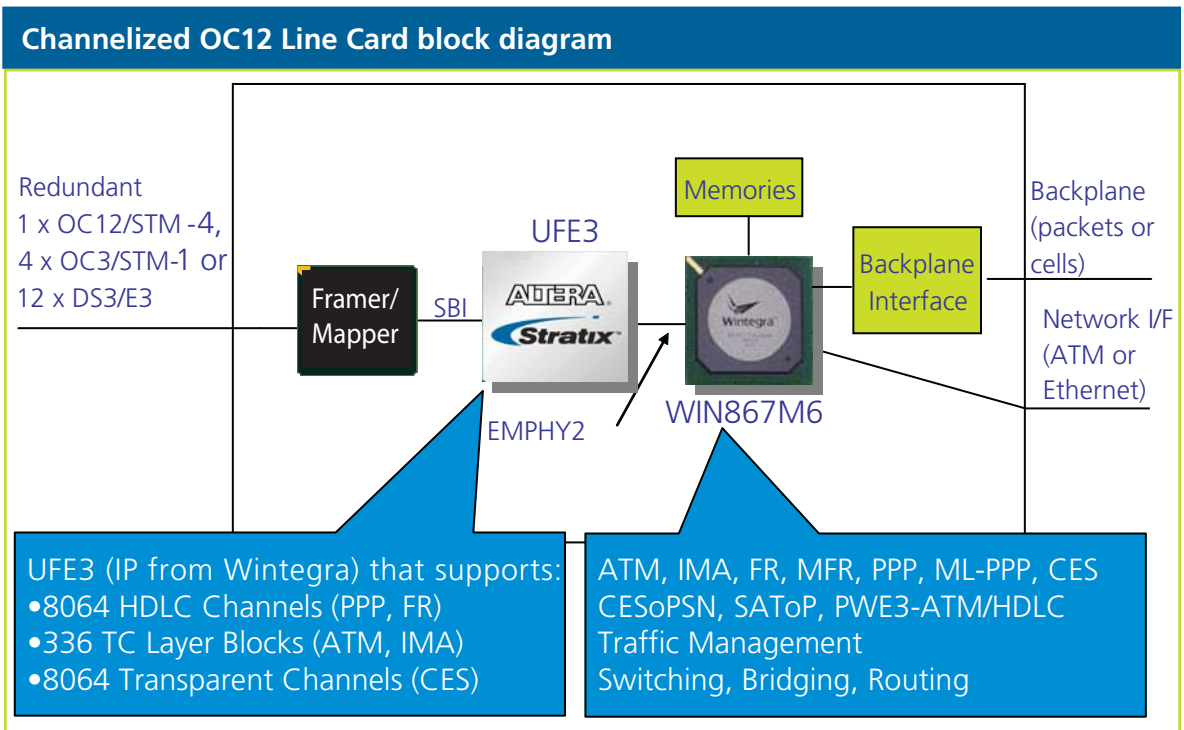
- 336 ports of IMA, ATM UNI, unstructured CES, SAToP (including clock recovery), PWE3-ATM
- 336 ports of Multi-link Frame Relay, or Multi-link PPP
- 8064 ports of FR, HDLC, PPP, structured CESoPSN, PWE3-HDLC with DS0, NxDS0, DS1 granularity
- Frame Relay to ATM interworking (FRF.5 and FRF.8.1)
- FRF.12 and Frame Relay Switching
- ATM or Packet Uplinks
- Fine grained traffic management

Wide Choice of Interfaces:

All WinPath2 devices are designed to accommodate all physical standards common to access equipment, including: T1, E1, J1, T3, E3, xDSL, OC-3 ATM, OC-3 POS, OC-12 ATM, OC-12 POS and 10/100 Ethernet. Gigabit Ethernet is supported externally through POS.

Scalable External Processing:

WinPath2 gives designers access to a scalable control path processing resource. Designers can choose either a device that includes an internal 64-bit MIPS core that operates at up to 600 MHZ , or opt for an external processor (such as the PowerPCTM 750). WinPath2 offers memory control functions on behalf of the external processor, so the PowerPC processor can be connected to the device gluelessly in cases where additional performance is required.



Simplified Systems Design:

To simplify design and allow customer cost savings, the WinPath2 fully integrates data path and control path, combining the functionality of communications processor and network processor into a single chip. This eliminates the external "bus" between data and control paths. In addition, WinPath2 offers a single integrated concept for buffer handling that simplifies the handoff between data path and control path.

WinPath2 Protocol Interworking:

WinPath2 provides designers the flexibility to achieve fast path application processing without control processor intervention. The Protocol Interworking diagram above shows a range of applications for which WinPath2 can be programmed to allow any of the four types of interfaces to interwork with any other. Full routing at the IP layer is supported with classification support to layer 4 or even multi-pass, multi-dimensional classification up to layer 7.

Since all data path protocols are simultaneously resident on-chip, this functionality can be instantly reconfigured. WinPath2's ability to dynamically balance four 250-350 MHz data path engines and four 200-350 MHz memory processors across the real-time characteristics of the multiple-rate data streams is a crucial feature for this device. This results in performance predictability matched only by custom ASIC designs. Whether an application needs 1 VC, 1 queue and 1 entry in the routing table, or 64K of each, the performance loading is nearly identical.

WinComm is programmed in a subset of the standard C language, which offers an excellent blend of the benefits of a high-level design environment with a performance-targeted compiler. Because of its modular design, new protocols can be added to the standard protocols resident with each chip.

WinPath2's protocols are available in a "ready-to-use" form (not reference code); it is similar to having several off-the-shelf standard peripherals integrated into a single chip. The device saves design time, since it can be quickly replicated across

a spectrum of board designs as different as IMA and Gigabit Ethernet, while also providing cost efficiency.

Wintegra Software Environment:

Utilizing one of over a hundred of Wintegra's example applications, a new system-specific device configuration can be programmed in just minutes. Wintegra offers best-in-class software integration and support through its WinPath Device Driver Interface (WDDI).

A networking API and a series of ANSI-C drivers make up the WDDI, which is production tested and field hardened for carrier-class demands.

WDDI is a host-based architecture that permits all configurable WinPath2 features to be accessed and managed via a standard ANSI C interface, with no loss of generality. Configuration and management are simplified by showing only user-definable fields. WDDI is a truly portable implementation with no RTOS or Board Support dependencies.

Additionally, a host registry is provided that allows tracking of specific WinPath configurations. Object oriented design allows WinPath based systems to be configured from the "bottom-up" yet managed from the "top-down" simplifying the overall software design.

Wintegra has worked with major RTOS providers and has ported VxWorks (Linux is under development) to its reference boards. Check with Wintegra for other porting schedules or use Wintegra's "roll your own BSP" development kit.

Additionally, reference implementations of ATM signaling stacks have been integrated with the WinPath API and drivers.

Performance:

With a few minutes of analysis, Wintegra can estimate device performance for its customers to a high degree of accuracy. Contact Wintegra for more information.

Supported Portocols	
Protocol	Function
ATM	
AAL0	Host Termination
	Interworking to Packet
AAL1	CES over TDM
	CES over EMPHY (1)
AAL2	CPS Host Termination & Switching
	SSSAR & SSTED Host Termination
	CPS Interworking to Packet
	SSSAR Interworking to Packet
AAL5	Host Termination and Interworking
Switching	ATM Cell Switching
IMA	Over TDM
	Over EMPHY (1)
	Over UTOPIA
OAM	Host Termination
	OAM-FM Support in Data Path
	OAM-PM Support in Data Path
Other	Multiple Queues per VC
	G.Bond
Packet	
Ethernet	Host Termination and Interworking
FR	Over TDM
	Over EMPHY (1)
	Switching and Interworking to ATM
MFR	Over TDM
	Over EMPHY (1)
HDLC/PPP	Multiple HDLC Channels per TDM
	Over TDM
	Over EMPHY (1)
ML-PPP	Over TDM
	Over EMPHY (1)
	PPP-Mux
PWE3	CESoPSN, SAToP over TDM
	CESoPSN, SAToP over EMPHY
Others	GRE
	GTP
	Header Compression (RFC2507/8/9)

Supported Protocols, cont'd.	
Protocol	Function
Interworking	
MPLS	Edge, Router
Routing	IPv4 Routing
	Dynamic Field Classifier
	NAT/PAT
Bridging	Bridging
	Dynamic Field Classifier
	VLAN stacking
Switching	Packet Switching
Others	Packet Policing
	WRED (routing)
	L4 Checksum
	L2/L3 Multicast
	ATM VC group hierarchical shaping
	System Egress backpressure

All Rights Reserved
 Printed in the United States of America
 All information contained in this document is subject to change without notice. The products in these documents are not intended for use in medical, life saving, or life support applications where malfunction may result in injury or death to persons. Wintegra may make changes to specifications or product descriptions at any time, without notice.
 The information supplied by this document is provided on an "AS IS" basis. In no event will Wintegra be liable for damages arising directly or indirectly from any use of the information contained in this document. Wintegra® is registered in the United States Patent and Trademark Office. For more information, see www.wintegra.com.
 UFE3PB- 0706- AM