

WinIP

IP-ONLY PRODUCT FAMILY

Highlights

- **Family of access processors with IP centric hardware and specific IP software support.**
- **Provides protocol processing required by IP networks such as encapsulation, IP Services, support for legacy services, Operation and Maintenance (OAM), Quality of Service (QoS) and Clock Synchronization.**
- **Carrier Grade, royalty free “production hardened” data path software supporting numerous IP protocols is included, plus C language API for rapid integration into high performance telecom systems.**
- **Advanced L2 protols available such as PWE3-SATOP, PWE3-CESoPSN, Ethernet G.Bond and RFC2507/8/9.**
- **RAM based Data Path code store to facilitate evolving standards.**
- **IP hardware support with 4 Gigabit Ethernet ports or up to 24 10/100 Mbit Ethernet ports.**
- **Hardare acceleration for functions like shaping, encryption support, and TDI clock generation.**
- **Powerful, scalable, data path processing elements (2, 4, or 6), all verisions are software compatible**

WinIP - Wintegra’s IP-Only Family of Access Processors

WinIP, Wintegra’s latest access processor family provides an IP focused hardware and software solution for evolving IP networks. The migration to all IP networks by carriers does not simplify the protocol processing requirements imposed on equipment providers. Simple Ethernet switches are not sufficient to provide advanced encapsulation such as MPLS, L2TP, GRE and Ethernet pseudo-wire, plus the Quality of Service (QoS) features such as shaping, policing and re-marking of IP packets needed by carriers to offer service level agreements (SLAs) with their customers. The WinIP family provides all of this protocol processing, and includes legacy support for TDM pseudo-wires and synchronization (clock recovery), all required by the evolving Metro Ethernet applications. WinIP devices are RAM based, which makes them field upgradable and provides superior product longevity since installed systems can be remotely modified to adapt to new standards.

Like other Wintegra access processors, the WinIP



family integrates both control and data path processing elements. These minimize system hardware complexity and facilitate the majority of the design effort to be on the application level software. The initial family members support up to 4 Gigabit Ethernet ports or 24 Fast Ethernet ports and can utilize DDR-I, DDR-II SDRAM and SRAM memories with ECC support. The WinIP devices also have on-board hardware accelerators for shaping, integrated encryption support as well as TDI clock generation circuitry. See the block diagram below.

The WinIP family of devices support:

Encapsulation:

- Providers Bridges
- Providers Backbone Bridges
- Ethernet pseudo-wires
- IPinIP

Services:

- E-LINE/VLL (Virtual Leased Line)
- E-LAN/VPLS (Virtual Private LAN Services)

Operation and Management (OAM) and Fault Management

- BFD, VCCV (Bidirectional Fault Detection, Virtual Circuit Connection Verification)
- Ethernet OAM (802.1ag (Continuity Check, Link Trace, Loop-back, Y.1731))

Quality of Service (QoS)

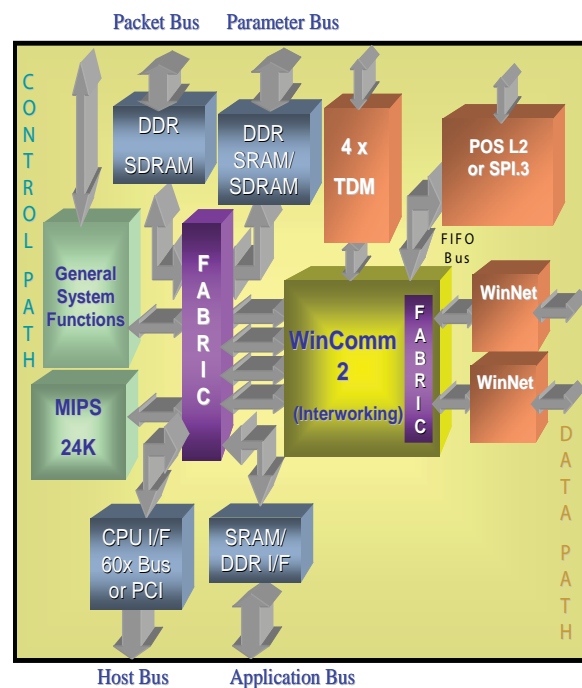
- Shaping
- Policing
- Classification
- Re-Marking
- Service Level Agreement (SLA) enforcement

Since Ethernet networks are generally asynchronous, the clocking information must be provided within the ethernet packets. WinIP supports the following synchronization methods:

- IEEE 1588v2
- Synchronous Ethernet
- GPS

Additional advanced Layer 2 protocols are also available such as various forms of pseudo-wires to transmit legacy connectivity over these IP networks. Customers can mix and match these protocols to suit their specific applications. Interfacing to customer

WinIP



WinIP Family Block Diagram

Data Path: (WinComm) up to 6 Processing Elements at 350 MHz

Control Path: MIPS 24Kc up to 600 MHz

System Interface Functions:

- On-chip PCI 2.2 interface
- Support for DDR-I, DDR-II SDRAM and SRAM with ECC support

Serial Interface

- Up to 4 GE or 24 FE
- POS L2 or SPI.3 (some derivatives)
- Support for 4 TDI (some derivatives)

Hardware Accelerators

- Special shaping hardware
- Integrated Encryption Acceleration
- TDI Clock Generation Circuitry

software is straightforward with Wintegra's supplied CG-WDDI (Carrier Grade- Wintegra Device Driver Interface).

The following protocols are available for the WinIP family. All of these are supplied with no cost or royalties.

Interworking:

- MPLS
- Bridging
- PB (VLAN Stacking)
- PBB (MAC in MAC)
- IPv4 Routing
- IPv6 Routing
- Packet/Switching
- Fast Re-Route
- Dynamic Field Classifier
- PPPoA/PPPoE
- IEEE 1588v2
- Synchronous Ethernet
- NAT/PAT
- Multicast
- PWE3 (Pseudo-wire End to End Emulation)
- GRE (Generic Routing Encapsulation)
- GTP (Generic Tunneling Protocol)
- L2TP (Layer 2 Tunneling Protocol)
- Programmable Header Manipulation (Remarking/Editing)

Quality of Service (QoS)

- Ethernet OAM (Operation and Management)
- BFD/VCCV
- Packet Classification
- Per-flow queuing
- Weighted Fair Queuing
- Hierarchical Shaping
- Packet Policing
- 2 Rate 3-Color Marking
- Host Termination
- Tail Drop
- Weighted Random Early Discard (WRED)
- Statistics/Billing

Layer 2 Protocols:

- Ethernet
- PWE3-CESoPSN (PWE3 Circuit Emulation over Packet Switching Networks)
- PWE3-SATOP (PWE3 Structured Agnostic TDM over Packet)
- IMA
- MC/ML-PPP (Multi-class and Mult-link Point to Point Protocol)
- MFR (Mult-link Frame Relay)
- ATM
- PPP/HDLC
- FR (Frame Relay)
- RFC 2507/8/9
- EFM G.Bond (Ethernet First Mile Bonding)
- Link Aggregation

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